

WHAT IS CLAIMED IS:

- 1 1. A method for determining a bit error rate in an input data stream
2 received on an integrated circuit, comprising:
3 determining over a plurality of first time intervals whether at least one
4 transition of the input data stream occurred in a predetermined phase
5 zone of a sample clock used to sample the input data stream; and
6 generating a count value according to how many of the first time intervals
7 have at least one transition that occurred in the predetermined phase
8 zone, the count value corresponding to the bit error rate.

- 1 2. The method as recited in claim 1 wherein the count value is generated
2 over a second time interval that includes the plurality of first time intervals.

- 1 3. The method as recited in claim 1 wherein determining the bit error rate
2 comprises:
3 generating a second count value over a third time interval that includes a
4 plurality of second time intervals, thereby providing better accuracy for
5 low bit error rates.

- 1 4. The method as recited in claim 1, further comprising supplying a bit
2 error rate indication corresponding to the count value via at least one output terminal
3 of the integrated circuit.

- 1 5. The method as recited in claim 4 wherein the bit error rate indication
2 supplied has a value that corresponds to a range of count values.

- 1 6. The method as recited in claim 4 wherein the bit error rate indication is
2 an analog signal supplied from the one output terminal of the integrated circuit, a
3 level of the analog signal indicative of the bit error rate.

- 1 7. The method as recited in claim 6 wherein the analog signal is a current.

- 1 8. The method as recited in claim 1 further comprising:

2 assigning a digital value that corresponds to the count value;
 3 supplying the digital value to a digital to analog converter;
 4 converting the digital value to an analog signal; and
 5 supplying on an output terminal of the integrated circuit the analog signal,
 6 thereby indicating the bit error rate according to a level of the analog
 7 signal.

1 9. The method as recited in claim 1 further comprising:
 2 asserting an output signal on an output terminal of the integrated circuit if the
 3 bit error rate is above a threshold value.

1 10. The method as recited in claim 9 further comprising:
 2 receiving an analog signal on an input terminal of the integrated circuit, a
 3 level of the analog signal indicative of the threshold value.

1 11. A method for determining if a phase-locked loop in an integrated
 2 circuit receiving an input data stream remains locked to a timing of the input data
 3 stream, the method comprising:
 4 determining over a plurality of first time intervals whether at least one
 5 transition of the input data stream occurred in a predetermined phase
 6 zone of a sample clock used to sample the input data stream;
 7 generating a count according to how many of the first time intervals have at
 8 least one transition that occurred in the predetermined phase zone; and
 9 evaluating whether the phase-locked loop remains locked to the timing of the
 10 input data stream according to the count.

1 12. The method as recited in claim 11 further comprising providing a
 2 signal indicating a loss of lock condition if the count exceeds a predetermined
 3 threshold.

1 13. An integrated circuit:
 2 means for detecting transitions of the input data stream occurring in a
 3 predefined phase zone of a sample clock sampling the input data
 4 stream; and

5 means for determining a bit error rate according to how many of a plurality of
6 evaluation intervals have one or more transitions in the predefined
7 phase zone.

1 14. The integrated circuit as recited in claim 13 further comprising:
2 means for supplying on an output terminal of the integrated circuit an
3 indication of the bit error rate, the indication corresponding to the
4 number of evaluation intervals that have one or more transitions that
5 fall into the predefined phase zone.

1 15. A method of determining a bit error rate of an input data stream,
2 comprising:
3 determining whether transitions of the input data stream fall into a
4 predetermined portion of a sample clock period of a sample clock
5 utilized to sample the input data stream; and
6 determining a bit error rate according to how many of a plurality of evaluation
7 intervals have one or more transitions in the predetermined portion of
8 the sample clock period.

1 16. The method as recited in claim 15, wherein the sample clock is a clock
2 recovered from the input data stream.

1 17. The method as recited in claim 15, wherein the determining includes
2 generating a count indicative of how many of the evaluation intervals have at least
3 one transition in the predetermined portion of the clock period, and supplying a bit
4 error rate indication corresponding to the count.

1 18. The method as recited in claim 17, further comprising converting the
2 count to a digital value corresponding to one or more count values.

1 19. The method as recited in claim 17 wherein the predetermined portion
2 of the clock period is adjacent to a clock edge used to sample the input data stream.

1 20. A method of making a tested integrated circuit comprising:

2 supplying an input data stream to the integrated circuit;
 3 determining whether transitions of the input data stream fall into a
 4 predetermined portion of a sample clock period of a sample clock
 5 utilized to sample the input data stream;
 6 determining how many of a plurality of evaluation intervals have one or more
 7 transitions in the predetermined portion of the sample clock period and
 8 supplying an indication thereof; and
 9 monitoring the indication to determine satisfactory performance of the
 10 integrated circuit.

1 21. The method as recited in claim 20 wherein the input data stream is
 2 supplied with varying data rates to test a frequency range of the integrated circuit.

1 22. The method as recited in claim 20 wherein the input data stream is
 2 supplied with varying amounts of jitter to test jitter tolerance of the integrated circuit.

1 23. An integrated circuit for receiving an input data stream, the integrated
 2 circuit comprising:
 3 a bit error detect circuit coupled to determine if a bit error occurs in the input
 4 data stream according to whether an input data stream transition occurs
 5 in a predetermined phase zone of a sample clock used in the bit error
 6 detect circuit; and
 7 a counter circuit coupled to the bit error detect circuit to supply an indication
 8 of a number of evaluation intervals in which at least one bit error
 9 occurs.

1 24. The integrated circuit as recited in claim 23 wherein:
 2 the bit error detect circuit includes a first data path and a second data path
 3 coupled to receive the input data stream, one of the first and second
 4 data paths being delayed with respect to the other, thereby defining the
 5 phase zone, and wherein respective output signals from the first and
 6 second data paths are coupled to a logic circuit to be logically
 7 compared.

1 25. The integrated circuit as recited in claim 23 wherein the first data path
2 is part of a phase detector circuit coupled to provide an indication of phase error
3 between a recovered clock being used to sample the input data stream and the input
4 data stream.

1 26. The integrated circuit as recited in claim 24 wherein the one of the first
2 and second data paths is delayed by delaying one of the clock and the data of the input
3 data stream supplied to the one path.

1 27. The integrated circuit as recited in claim 23 wherein the second data
2 path includes one or more selector circuits to select from a plurality of clock
3 frequencies.

1 28. The integrated circuit as recited in claim 24 wherein the respective
2 output signals from the first and second data paths are logically compared in an
3 exclusive OR circuit.

1 29. The integrated circuit as recited in claim 23 further comprising:
2 an output terminal supplying a digital signal indicative of a bit error rate, the
3 output terminal being part of a communication port, the bit error rate
4 being determined according to how many of the evaluation intervals
5 have at least one bit error.

1 30. The integrated circuit as recited in claim 23 further comprising:
2 an output terminal supplying an analog signal indicative of a bit error rate, the
3 bit error rate being determined according to how many of the
4 evaluation intervals have at least one bit error.

1 31. An integrated circuit for determining an out-of-lock condition with
2 respect to an input data stream, the integrated circuit comprising:
3 a phase zone detect circuit coupled to determine if a transition of the input data
4 stream occurs in a predetermined phase zone of a sample clock used to
5 sample the input data stream;

6 a counter circuit coupled to the phase zone detect circuit to supply a count
 7 indication of how many of a predetermined number of evaluation
 8 intervals have at least one transition that occurs in the predetermined
 9 phase zone; and
 10 a compare circuit coupled to compare the count indication to a predetermined
 11 value to determine if a phase-locked loop remains locked to a timing of
 12 the input data stream.

1 32. The integrated circuit as recited in claim 31 wherein each of the
 2 evaluation intervals comprises multiple bit times of the input data stream.

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